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An Efficient Design of Low Power Sequential Circuit Using Clocked Pair Shared Flip Flop

D. Mahesh Kumar
Assistant Professor – *Department of Electronics, PSG College of Arts & Science, Coimbatore – 641014, India.*

Dr. R. Kannusamy
Head – Department of Electronics, PSG College of Arts & Science, Coimbatore – 641014, India.
E-mail:Mahesh.research01@gmail.com

Abstract
Power consumption plays an important role in any of the integrated circuit and is listed as one of the most important top three challenges in the international technology roadmap for semiconductors. In any type of integrated circuit, clock distribution network and flip –flop consumes large amount of power because they make and employ maximum number of internal transitions. In the clock distribution network, the clock signal distributes from a common point to all the elements that needed for the circuit. However this function is more important to the synchronous system, much attention has to give to the characteristics of these clock signals. In the synchronous system, a clock distribution network consumes a large amount of total power because of the high operation frequency of highest capacitance. An effective way to reduce the capacity of clock load is by minimizing the number of clocked transistor. Clock distribution networks consumes a large amount of chip power in a low swing differential capturing flip flop system and also it creates a more number of clocked transistor. But by using the proposed system, the clocked paired shared flip flop is used to reduce the number of local clocked transistors.

Keywords: Low swing differential capturing flip flop; Clocked transistor; Pass transistor, Transmission gates

INTRODUCTION

In many VLSI chips, the total chip power consumption will occur with the power dissipation in the clocking system, including clock distribution network and flip-flops. This type of design is to use more pipeline stages for high throughput, which will increase the number of flip flops in a chip. Thus, it is very important to reduce the power consumption in both the clock trees and the flip-flops. VLSI is the main field which involves packing more and more logic devices into smaller and smaller size areas. But in the recent years, there is an increasingly giving importance to the power is being given similar importance same as the area and the speed. The clock network constitutes one of the most important segments of a synchronous VLSI chip as it can significantly influence the speed, area, and power dissipation of the system. Generally there are four different sources of power dissipation in digital CMOS circuits. They are: switching (or dynamic) power, short-circuit power, leakage power, and static power.

The physical design of a chip is built on a hierarchy of transistors, macros, units and microprocessor cores. In that three types of macros are employed and they are custom, SRAM and synthesized. During the high-level design phase of process, the macros, units, core and chip are all assigned contracts for timing, area, shape, wiring tracks and I/O. Timing and physical design of the chip are done concurrently on all the levels of the hierarchy. All major buses are routed early in the design.

During the last decade, extensive considerations and importance have been given to the use of pass-transistor logic networks in the implementation of digital systems. To reduce the power consumption in clock distribution networks, several small-swing clocking schemes have been proposed and their potential for practical applications has been shown [3], [4]. The previous half-swing scheme requires four clock signals and in that it suffers from skew problems among the four clock signals and requires additional chip area [4]. To reduce the leakage current [3] a reduced clock swing flip-flop (RCSFF) is used additionally for high power supply voltage. A single-clock flip-flop is used for half swing clocking and does not need high power-supply voltage but has a long latency [2].

The hybrid-latch flip-flop (HLFF) and semi dynamic flip-flop (SDFF) have been known as the fastest FFs, but they consume large amounts of power due to redundant transitions at internal nodes [5]–[7]. To reduce the redundant power consumption in internal nodes of high-performance flip-flops, the conditional capture flip-flop (CCFF) has been proposed [8]. However, for the clock tree the HLFF, SDFF, and CCFF use full-swing clock signals that cause significant power consumption. The focus of this work is to develop a unified method for mapping logic functions into circuit realizations using different pass-transistor logic styles. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications.

EXISTING SYSTEM-A LITERATURE SURVEY

Seyed E. Esmaeili Rttl. *et al* has proposed conditional capturing which can be used to minimize the power at low data switching activities by means of eliminating redundant internal transitions. This is done because to reduce the short

circuit power. The load pMOS transistor in the reduced swing inverters is always in saturation since Vgs=Vds and also it lowers the voltage at the source of the second pMOS in each inverter to approximately VDD-|Vtp| thus turning it off when the low-swing sinusoidal clock signal reaches its peak voltage.

S.E. Esmaeili A.J. Al-Khalili G.E.R *et al* explains the differences in the results for the response of the dual edge triggered flip-flop obtained from the schematic and at the post-layout simulations. When inverted using an inverter, the resonant sinusoidal clock signal becomes a square wave clock. The effect of the long rise time of the positive edge of the sinusoidal clock signal CLK1, which defines the start of the first evaluation interval TE1, compared to the effect of the short rise time of the inverted square signal CLK2, which defines the start of the second evaluation interval TE2, on the TDQ delay against TDCLK delay is also investigated.

Chulwoo Kim, *et al* Member, IEEE has designed a schematic of our LSDFF composed of a data-sampling front end and data-transferring at the back end. In the internal nodes X and Y are charged and discharged according to the input data Din, not by the clock signal. Therefore, internal nodes of LSDFF switch only when the input changes. LSDFF does not require a conditional capture mechanism, as used in the pulse-triggered true-single-phase-clock (TSPC) flip-flop (PTTFF). In PTTFF, either one of the data-precharged internal nodes is in floating state, which may cause malfunction of the flip-flop. Also, its internal node does not have a full voltage swing, which causes performance degradation.

Hamid Mahmoodi, *et al* has designed the conventional energy recovery clocked flip-flop and it consists of a four-phase transmission-gate (FPTG) flip-flop. FPTG is similar to the conventional transmission gate flip-flop (TGFF) except that it uses four-transistor pass-gates designed to conduct during a short fraction of the clock period. The main disadvantage of this flip-flop is it needs the four sinusoidal clock signals and has the long delay. Transistors will be required for the pass-gates are large, resulting in large flip-flop area. Another approach for energy recovery clocked flip-flop is to locally generate square-wave clocks form a sinusoidal clock.

PROPOSED SYSTEM

- Clock pair shared flip flop (CPSFF) is used in the clock distribution networks.
- Number of clocking transistors is less when compared to the low swing differential conditional capturing flip flop.
- Hence it consumes low power with less area.

Circuit Diagram :

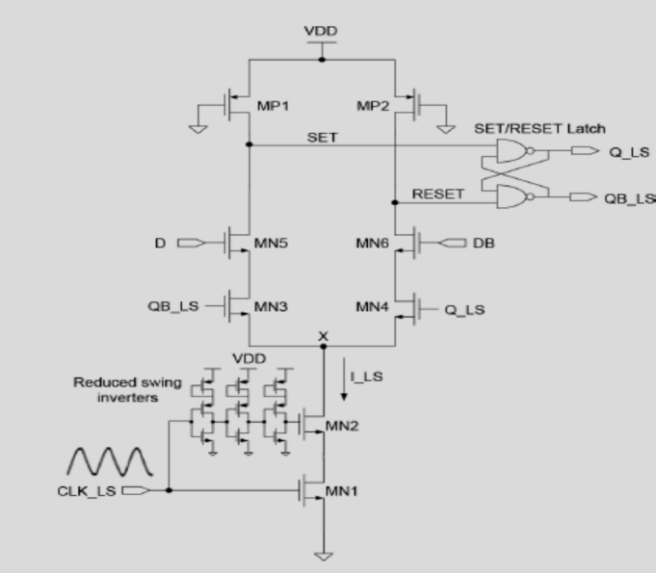

Figure 1: LS-DCCFF

Low-swing differential conditional capturing flip-flop (LS-DCCFF) [1] operates with a low-swing sinusoidal clock during the operation of reduced swing inverters at the clock port. By means of a low-swing differential conditional capturing flip-flop (LS-DCCFF) for use in low-swing LC resonant CDNs. This is the first application of low-swing clocking to LC resonant CDNs. Low-swing clocking would normally require two voltage levels. These voltage levels can be generated using one of two schemes: (1) dual-supply voltages and (2) regular power supply. The first scheme adds circuit and extra area complexity to the overall chip design and layout. In adding, it is easy to construct double edge triggering flip-flop based on the simple clocking structure in CPSFF. Additional CPSFF could be used as a level converter flip-flop automatically, because incoming clock and data signals only drive nMOS transistors.

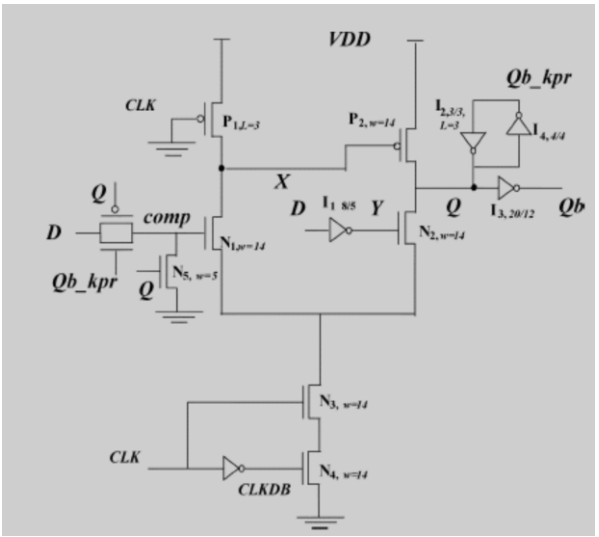

Figure 2: Clocked pair shared flip-flop.

In this CPSFF, high swing and floating values were obtained and at the same time the output is not properly obtained. Due to the clock input as square wave there is a high output swing in this circuit. For that purpose resonant circuit (inverter stage) is used to overcome this drawback and some modification has been done. Here LS-DCFF is the proposed system of this paper, in which sine wave is applied as input to reduce the high output swing. By using this method the transistor count is also reduced. To reduce the power consumption of the proposed CSPFF circuit it is proposed to use modified pass transistor logic which reduces the transistor count also. Hence both the proposed (CSPFF) and proposed-d (CSPFF with Pass transistor Logic) techniques has been designed.

There are two main pass-transistor circuit styles: those that use NMOS only pass-transistor circuits, like CPL [11], and those that use both NMOS and PMOS pass-transistors, DPL [9] and DVL [10]. Complementary pass-transistor logic [11] consists of complementary inputs/outputs, a NMOS pass-transistor network and CMOS output inverters. The circuit function is implemented as a tree consisting of pull-down and pull-up branches. Since the threshold voltage drop of NMOS transistor degrades the "high" level of pass-transistor output nodes, the output signals are restored by CMOS inverters. CPL has traditionally been applied to the arithmetic building blocks [11–13] and has been shown to result in high-speed operation due to its low input capacitance and reduced transistor count.

To avoid problems of reduced noise margins in CPL, twin PMOS transistor branches are added to N-tree in DPL [9]. This addition results in increased input capacitances. However its symmetrical arrangement and double-transmission characteristics compensate for the speed degradation arising from increased loading. The full swing operation improves circuit performance at reduced supply voltage with limited threshold voltage scaling.

The main drawback of DPL is its redundancy, i.e. it requires more transistors than actually needed for the realization of a function. To overcome the problem of redundancy, a new logic family, DVL [10, 14], is derived from DPL. It preserves the full swing operation of DPL with reduced transistor count. As introduced in [10], DVL circuit can be derived from DPL circuits in three steps.

Application :

- Low power application in deep submicron circuits
- In future mobile Systems for low leakage & enhanced battery efficiency.
- Registers
- Counting purpose
- Single bit storage device
- Timing operation
- Frequency division
- Parallel data storage

COMPARISON OF POWER-SAVING APPROACHES

Among other logic style, the CPSFF pass-transistor logic style, proves to have the best performance values and lowest power-delay products. Only the single-rail style of LEAP is a viable alternative if lower power and compatibility with cell-based design are of concern. The advantages of efficient circuit and layout implementation of simple gates, the absence of swing restoration circuitry, and the single-rail logic property are predominant in most circuit applications.

We have described the power-saving approaches of several conventional flip-flops and the proposed CSPFF in the previous sections. In this section, we will summarize the different approaches to reduce the power consumption of the clocking scheme. First, CSPFF reduces the power consumption of LSDFF by removing redundant internal data holding node switching. Second, small-swing clock flip-flops reduce the power consumption in the clock network by reducing the clock voltage swing. Also, the capacitance of the clocked transistors of the FF is also reduced in CSPFF. Finally, CSPFF uses both a low-swing clock and a double-edge triggered operation to reduce power consumption in the clock network. Further, CSPFF does not have any redundant internal data holding node switching. Table I summarizes power-saving approaches in each flip-flop.

Table I: Comparisons of Flip-Flop

	No. of Transistor	**No. of Clked Transistor**	**Power (μW)**	**Power Dissipation**
LSDFF	28	3	132	26.3
CPSFF	22	2	116	19.4
CPSFF with Pass transistor Logic	18	2	110	14.2

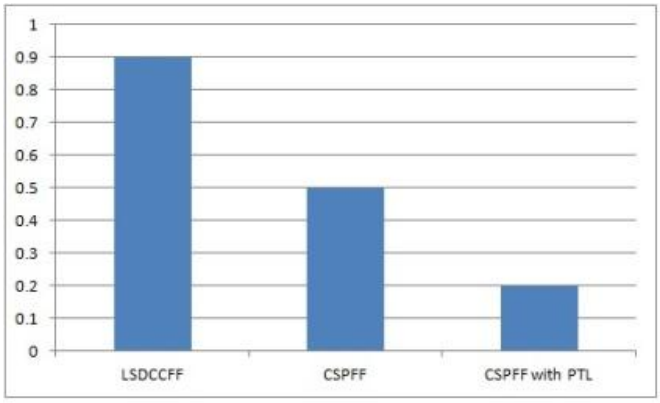

Figure 3: Clock network power consumption comparisons.

IMPLEMENTATION RESULTS

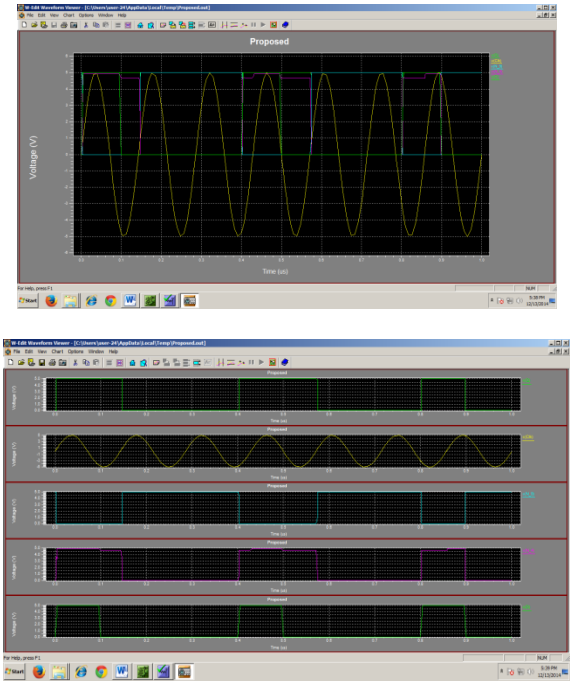

Figure 4(a): Simulation Output of LS-DCCFF

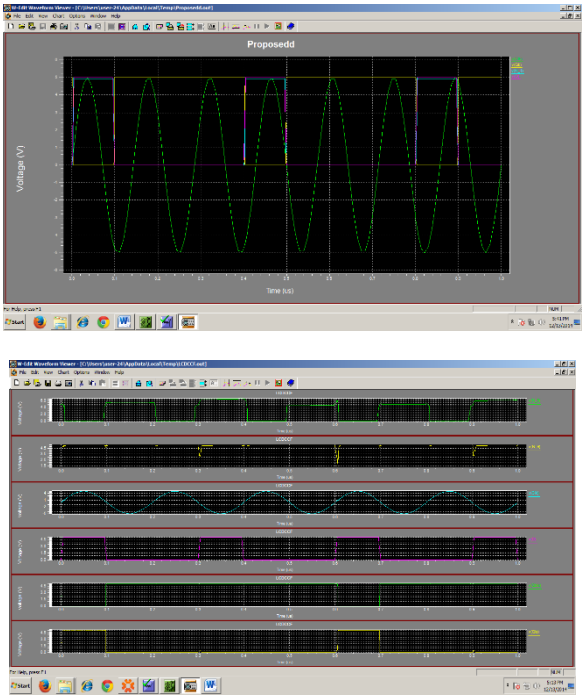

Figure 4(b) Simulation Output of proposed method (CPSFF)

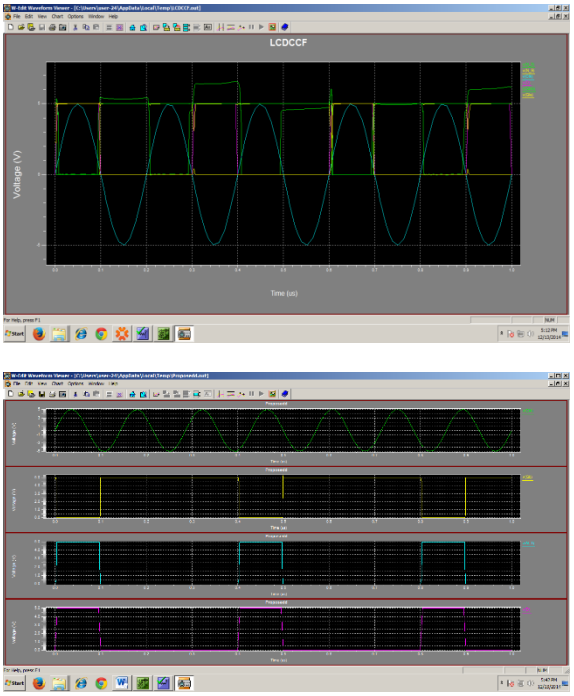

Figure 4(c): Simulation Output of CSPFF with Pass Transistor Logic

We have analyzed several conventional flip-flops and have developed a new flip-flop in a 0.18-µm CMOS process. Each flip-flop is optimized for power-delay product. The low-swing clock voltage for LSDFF was about 1 V. The output load capacitance was assumed to be 100µF. The simulated waveforms of the LSDFF are shown in Fig. 4(a). Comparisons of simulation results for the two FFs are summarized in Table I. As Fig. 3 shows, CSPFF-PTL has the least power consumption when the input pattern does not change, whereas LSDCCFF and CSPFF still incur high power consumption even though the input stays 1. For an average input switching activity of 0.3, the power consumption of CSPFF-PTL is reduced by 25.6% -44.6% over conventional FFs.

CONCLUSION

In our investigations, a low-swing clock shared paired flip-flop (CSPFF with PTL) has been developed in a 0.18 µm dual- CMOS process to the reduce power consumption in both the clock trees and the flip-flops. The CSPFF-PTL inherently avoids unnecessary internal node transitions. Furthermore, CSPFF-PTL uses a double-edge triggered operation as well as a low-swing clock, which reduces power consumption in the clock tree. The overall power saving of CSPFF is significant over conventional high-performance flip-flops with comparable D-to-Q delay. Also, an additional 78% power saving is achieved in the clock network. The negative setup time of CSPFF-PTL helps to overcome the clock skew problems. With simple logic embedding, CSPFF-PTL reduces overall delays within a pipeline stage.

CMOS also compares favorably with regard to circuit speed and layout efficiency. Its single-rail property is crucial for saving routing resources, which is an important issue in

submicron VLSI. Its robustness against transistor downsizing and voltage scaling allows the efficient power optimization of noncritical signal nets and of entire circuit components. As a matter of fact, circuit robustness is becoming a key aspect in deep-submicron VLSI, where variation ranges of many process and environment parameters will increase massively. This, together with its ease-of-use, makes complementary CMOS the logic style of choice for low-power, low-voltage implementation of arbitrary combinational circuits and for design automation—i.e., low-power synthesis and cell-based design—, also and particularly in the future [10]. However, other logic styles, such as CPL, may still be viable candidates for low-power high-speed implementation of dedicated circuit applications like multipliers.

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Authors Biography

D. Mahesh Kumar obtained his B.Sc., Electronics and M.Sc., Applied Electronics from PSG College of Arts and Science, Coimbatore in 1996 and 1998 and also M.Phil., in Electronics from PSG College of Arts and Science, Coimbatore in 2006. He has been working in the teaching field for about 16 years. His area of interest includes VLSI Design, Wireless Communication and Embedded System. He has published many articles in the reputed national and international journals and also one book on the topic "Textbook of Operational Amplifier and Linear Integrated Circuits" by Macmillan India Ltd., New Delhi.

Dr. R. Kannusamy obtained his B.Sc., Physics from Kandasamy Kandars College, Velur (Namakkal Dt.,) in 1982 and M.Sc., Physics from NGM College, Pollachi in 1984 and also M.Phil., in Physics from Bharathiar University, Coimbatore in 1986. He completed Ph. D., in the year 2009. He has been working in the teaching field for about more than 25 years. He has published many articles in the reputed national and international journals.