AENSI Journals

Australian Journal of Basic and Applied Sciences

ISSN:1991-8178

Journal home page: www.ajbasweb.com

A Review on Test Pattern Generation for Low Power Built In Self Test Application

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ARTICLE INFO

Article history:
Received 25 June 2014
Received in revised form
8 July 2014
Accepted 25 August July 2014
Available online 29 September 2014

Keywords:
Built-in-Self-Test (BIST), Test Pattern Generator (TPG), Linear Feed Back Shift Register (LFSR), Multiple Single Input Change (MSIC), GBM.

ABSTRACT

Background: Background: Modern manufacturing techniques in IC design are growing such that the transistor count on a single chip escalates exponentially with complex Embedded and DSP cores in it. Consequently, testing of such complex ICs are remarkably challenging. In this paper we consider the implementation of parallel test patterns generation which is used as a basic building Block in built-in-self test (BIST) design. It is a well-known fact that test power is several times higher than functional power. **Objective:** This paper first gives an overview of the need and importance of low power testing and the various methods for test pattern generation. **Results:** The proposed Test pattern generator (TPG) can drive several circuits under test (CUT) within a complex VLSI IC and it outperforms the existing counterparts in providing an efficient and effective way in greatly reducing power consumption, delay and complexity. A comparison of, newly developed test solutions with respect to key parameters of low power testing like, test power, delay and so on is presented for choosing a best possible solution. This proposed method utilizes GBMAC (Galois field based multiply and accumulate) units, which consist of Galois based Finite field Multipliers and several accumulators, in DSP to generate test patterns. **Conclusion:** Hence the new method can generate test patterns without LFSRs (linear feedback shift registers) and Multiple Single Input Change (MSIC). Fine review in any research area is crucial for well again Perceptive of its fundamentals and it also indicates the trends and scale for potential research in the special area**.**

To Cite This Article: D. Mahesh Kumar and Dr.R. Kannusamy., A Review on Test Pattern Generation for Low Power Built in Self Test, ***Aust. J. Basic & Appl. Sci.,*** *8(15): 77-84, 2014*

INTRODUCTION

Today's VLSI ICs are racing towards reduced area, highly complex and high speed circuits as predicted by Moore (B. Chappell, July 1999). As the VLSI designs increase in the integration density, associated modules becomes inaccessible and testing of the chip becomes more challenging. For higher speed and low-power consumption still VLSI processors are so in demand. There are many types of problems facing by the test industries like increase in test time and test volume Tomovska,J., S, Presilski., N, Gjorgievski., N, Tomovska., M.S. Qureshi and N.P. Bozinovska., 2013.Development of a spectrophotometric method for monitoring angiotensin-converting enzyme in dairy products. Pak Vet J, 33(1): 14-18.

When external ATE is employed for testing. In general, combinational circuits are not pseudo exhaustively testable and so there a deterministic test sets have to be applied, if the circuit is not allowed to be segmented by test points for timing or area reasons. Earlier DFT (Design for Testability) techniques are concentrated on fault coverage, test length, test application time and test quality. Today's ATPG (Automatic Test Pattern Generator) tends to produce less test patterns only and also it cannot cover most of the test scenarios. Apart from this these test pattern produces number of internal nodes switching. (As shown in the Fig.1.)

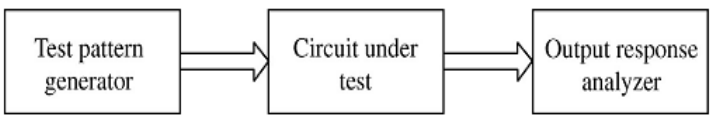

Fig. 1: BIST Configuration.

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The most important role of the test pattern generator is to relate test patterns to the circuit under test (CUT). The output response analyzer is analyzed from the resultant output patterns as shown in the figure 1. Ideally, a BIST scheme is effortless to implement and must provide high fault coverage. When test pattern is applied to CUT (Circuit under Test) a number of nodes switching happens and also the correlation between two test vectors are very less. The test generation module that has been widely used in BIST design is the linear feedback shift register (LFSR).). Linear Feedback Shift Registers (LFSR) are extensively used in BCH encoders and CRC operations .LFSRs are also Used in conventional Design for Test (DFT) and Built-in Self-Test (BIST) and LFSRs are used to carry out response compression , while for the DFT, it is a foundation of pseudorandom binary test sequences. The implementation of LFSR is done in hardware .(P. Girard, L. Guiller, C. Landrault, S. Pravossoudovitch, J. Figueras, S. Manich, P. Teixeira, and M. Santos, Jul. 1999 and Saraswathi, T., Ragini, K., Reddy, C.G.,Jan 2011) due to the ease of construction from simple electromechanical or electronic circuits, long periods, and very uniformly distributed output streams. However, an LFSR is a linear system, leading to fairly easy cryptanalysis. A sequential LFSR circuit cannot meet the speed requirement when high-speed data transmission is required. a new test pattern generation method using the processing units of DSP (digital signal processing). This proposed method utilizes GBMAC (multiply and accumulate) units, which consist of multiplier and several accumulator, in DSP to generate test patterns. Multiplier has a seed value and performs a Galois based Multiplication. In order to generate pseudo random test patterns the addition of two products is done in accumulator. Consequently, block can be analyzed by using a mixture of test-pattern combinations helps to Decreasing power consumption, area overhead and delay that are associated with sequential circuits. This is because the proposed circuit doesn't use pipeline registers that are triggered by a system clock and consumes much power. The rest of the paper is organized as follows. Describes related works in the test vector selection. Besides it describes our test selection technique with the experimental results. Finally, conclusion of the paper with future contribution.

Conventional Methods:

Exhaustive Testing:

The first method is the exhaustive testing method and in that, all feasible input patterns are apply to the CUT i.e. intended for an n-input combinational circuit, all possible 2^n patterns are needed to be applied. The advantage of this method is that all non-redundant faults can be detected but a bridging fault cannot be detected. The disadvantage of this method is when *n* is large, the test application time becomes excessive, even with high clock speeds. Thus, exhaustive testing is suitable only for the circuits with a partial number of inputs. The second method is that a slight modification has been done in the previous exhaustive testing and is so called the pseudo exhaustive testing (Bo Ye., Tian-wang Li., July 2010). It has the identical advantages of exhaustive testing while considerably dropping the number of test patterns to be useful. The basic idea in the pseudo exhaustive testing is to partition the circuit under test into several sub-circuits. In that, each sub-circuit has few adequate inputs is available for the exhaustive testing is to be handled for it. This concept has been used in autonomous design verification procedure. To illustrate the use of this type of technique, let us consider the circuit shown in Fig.2.

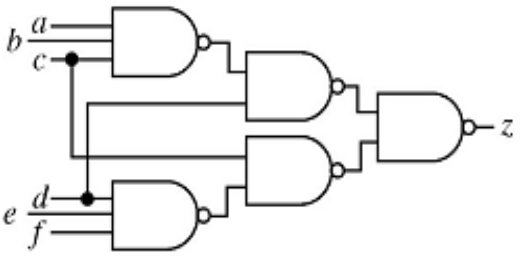

Fig. 2: Circuit under Test [CUT].

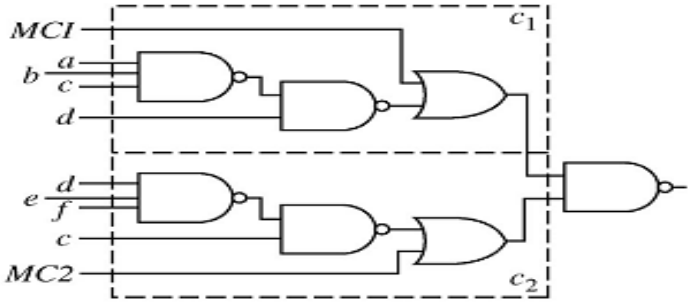

Fig. 3: Two Sub-circuits.

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In that (Fig.3) Partition sub-circuits C1 and C2 as shown in Figure 2b. The function of the two control inputs MC1 and MC2 are as follows; when MC1=0 and MC2=1, the sub-circuit C2 is disabled and the sub-circuit C1 is enabled, that can be tested by applying all possible input combinations at a, b, c, and d. Similarly, when MC1=1 and MC2=0.Finally, when both the MC1=0 and MC2=0, the circuit functions has need not to be modified except for the added gate delay. The advantage of this style is to analyze the any fault in the circuit itself and also the testing circuit is detectable.

Related work:

Huoy-Yu Liu ,San Diego, Chung-Kuan Cheng, 2013, proposed Pseudo-exhaustive testing (PET) offers a simple solution to testing complex circuits and systems. However, PET suffers long testing time for test generation and high area overhead of test hardware. The pipelined pseudo-exhaustive testing (PPET) achieves fast testing time with high fault coverage by pipelining test vectors and test responses among partitioned circuit segments. To reduce hardware overhead in PPET, a novel approach for implementing area-efficient PPET is presented. ***Linear Feedback Shift Register (LFSR).***

During BIST, it is important that the circuit be excited once and only once with a particular pattern. This is due to a given pattern causes an error vector to appear at the faulty circuit outputs, which are read by the BIST response compactor, and repeating the pattern later cause the same error vector to be appear again. Since the response compactor is an XOR-ing system as well, the two erroneous responses from that error vector will cancel and leave the BIST system with only the good machine response. As a result, this causes the testing hardware to accept a faulty circuit as a good circuit.(Chand, S.R.., Srinivas, Sai, T.V. Sailaja, M.Madhu,T.,Dec 2010).(C. K. Koc and T. Acar, August 1996 and C. Laoudias and D. Nikolos, Apr. 2004) analyzed the impact of a linear feedback shift register (LFSR) is a shift register whose input bit is a linear function with respect to early state. The generally used linear function of a single bit is X-OR gate. The LFSR consists of D flip-flops and exclusive-OR (XOR) gates as the feedback network which feeds externally from X_0 to X_{n-1}. Thus, shift register in an LFSR is mainly driven by the X-OR gate of some bits of the overall shift register value thus forming a feedback loop. In this technique, the bits controlled in certain positions in the shift register

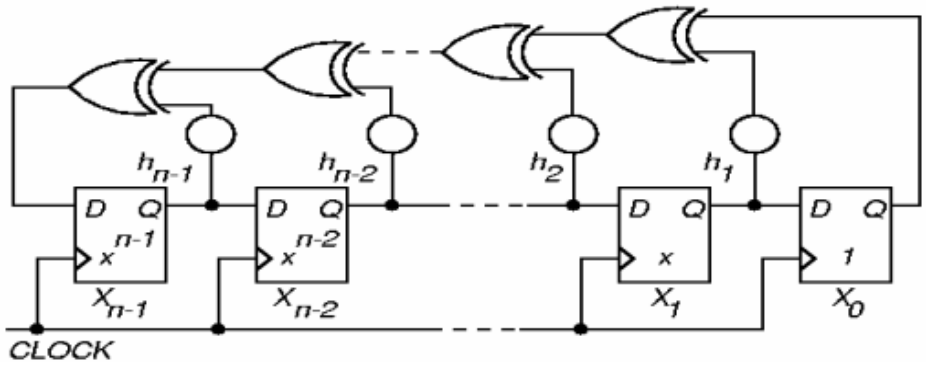

Fig. 4: Linear feedback shift register.

Are in several sort of function and the outcome is fed back into the register's input bit. After that the certain bit values are collected before the register is clocked and the result of the feedback function is inserted into the shift register during the shift and filling the position that is emptied as a consequence of the shift. The bits position is used in the feedback function are called "taps". The lists of the taps are called the "tap sequence". The output bit of an LFSR is i.e. n-bits long is the nth bit and the input bit of an LFSR is bit 1. The state of an LFSR that is n-bits long can be any one of 2n different values. The largest state space likely for such an LFSR will be 2n – 1, all promising values except the zero state. All zero is not allowed in the LFSR as it will always produce zero in spite of how many clock iteration. Because each state can have only once following state, an LFSR with a maximal length tap sequence will pass through every non-zero state once and only once before repeating a state. (N. Basturkmen, S. Reddy, and I. Pomeranz, Sep. 2002 and P. Girard, May–Jun. 2002) (Fig.4 shows a general structure of conventional LFSR.)

Related work:

The author Yi Wang and Gui-Juan Xu 2012 , proposes random single input change test vector generator and configurable 2D LFSR. The proposed method reduces the switching of internal nodes of CUT and raises correlation between test vectors in a sequence. It is suitable for BIST.

Solecki, J. et al. 2013 ,presents new LFSR that derives appropriate phase shifter and produces a binary sequence with low switching activity without compromise in test coverage and test application time.

Multiple Single Input Change (MSIC):

(F. Corno, M. Rebaudengo, M. Reorda, G. Squillero, and M. Violante, Apr.–May 2000 and Feng Liang, Luwen Zhang, Shaochong Lei, Guohe Zhang, Kaile Gao, and Bin Liang, April 2013)MSIC is a test pattern generator (TPG) method that can change an SIC vector to exclusive low transition vectors for multiple scan chains [2]. In this process first, the SIC vector is decompressed to its multiple code words and the generated code words will bit-XOR with a same seed vector in turn.

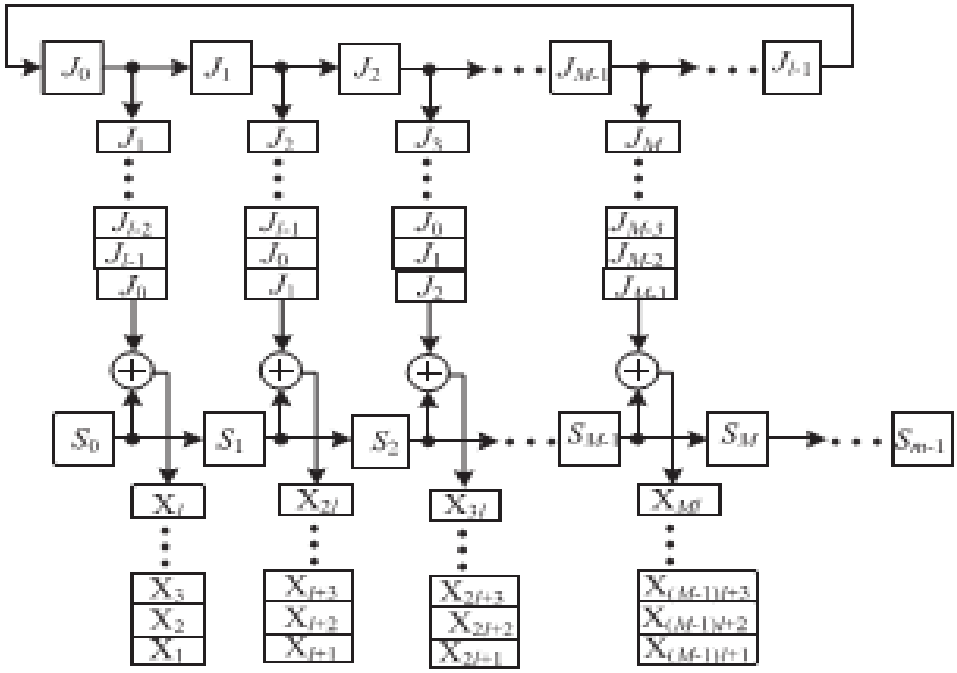

Fig. 5: Symbolic simulation of an MSIC pattern for scan chains.

The architecture consists of SIC generator, a seed generator, an XOR gate network, a clock and control block. Assume that there are m primary inputs (PIs) and M scan chains in a full scan design and in that each scan chain has z scan cells. Fig.5 implies the representative simulation for one generated pattern.

i)The primitive polynomial is $S(t)=S_0(t)S_1(t)S_2(t),...,S_{m-1}(t)$ and

ii)the vector generated l-bit Johnson counter is $J(t)=J_0(t)J_1(t)J_2(t),...,J_{z-1}(t)$.

iii) At first clock $J = J_0J_1J_2,...,J_{z-1}$ bit-XOR $S = S_0S_1S_2,...,S_{M-1}$, and

iv) The output is $X_1X_l+1X_{2l}+1,...,X_{(M-1)}l+1$

v) At second clock cycle, $J = J_0J_1J_2,...,J_{z-1}$ is shifted circularly as $J =J_{l-1}J_0J_1,...,J_{z-2}$, XOR $S=S_0S_1S_2,...,S_{M-1}$.

vi) The output is $X_2X_l+2X_{2l}+2... X_{(M-1)l}+2$.

Related work:

Feng Liang, Luwen Zhang, Shaochong Lei, Guohe Zhang, Kaile GAO, and Bin Liang, 2013, proposed TPG is flexible to both the test-per-clock and the test-per-scan schemes. A theory is also developed to symbolize and analyze the sequences and to take out a class of MSIC sequences. Investigation results show that the created MSIC sequences have the favorable characteristics of standardized distribution and low input transition density.

All the previous test pattern generating methods which we have dealt with consists of two or more flip-flops thus consuming power greatly, area and delay. Hence power consumption is reduced by our proposed technique. It comprises only less number of transistors which in turn reduces the area overhead. Moreover it is a high speed circuit and operates in GHz. The parallel architecture of the proposed circuit also contributes to the increase in speed of pattern generation

Proposed Method:

Latest DSPs have a special unit called GBMAC. The GBMAC unit consists of a multiplier and an accumulator and performs multiplication and accumulation simultaneously. Some DSPs have two or more GBMAC units to increase the performance. As compared with the accumulator-based TPG method, the GBMAC-based TPG method utilizes multiplication, an addition, and accumulation. Through the multiplication, a greater variety of sequences of test vectors can be generated. Fig.6 shows the structures of the main GBMAC-

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based TPG schemes for single GBMAC. Fig.6 (a) Implies a seed-multiply and accumulate unit and Fig.6 (b) Implies a seed-multiply and add combined accumulate unit. The seeded multiply and accumulate scheme is a basic method for a GBMAC-based TPG and it has a simple generation process. Here the proposed GBMAC unit performs modular multiplication without division. The algorithm is also proven accurate in Finite Fields arithmetic Instead of a(x)b(x)modf(x) the algorithm calculates $a(x)b(x)r^{-1}(x)$ mod f(x) where r(x) is a precomputed value. It is required that gcd(r(x), f(x)) = 1. By choosing $r(x) = x^k$. For the gcd(r(x), f(x)) = 1 assumption to hold, it suffices f(x) not be divisible by x, which is always the case since f(x) is defined over the field GF (2). Through the correct choosing of the value r(x), the algorithm becomes less complex and can give efficient hardware implementations. So for $r(x) = x^k$ the bit level algorithm (Manohar Ayinala and Keshab K. Parhi, Sep. 2011 and M. Nourani, M. Tehranipoor, and N. Ahmed, Mar. 2008) has the Following methodology.

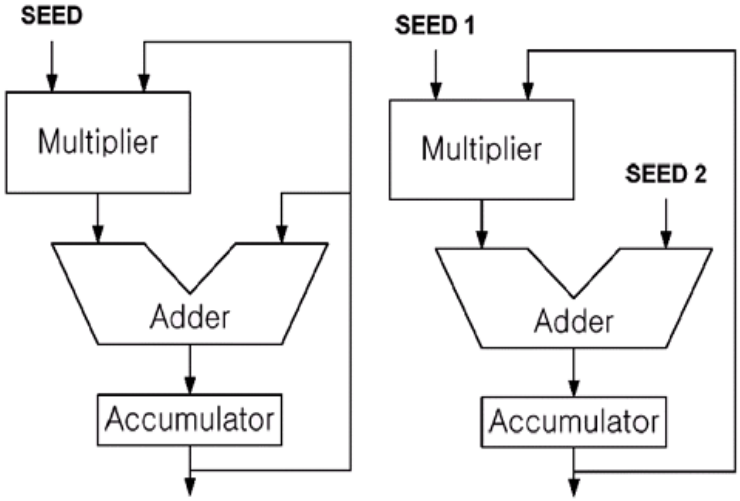

Fig. 6 :(a) Seed-multiply-Accumulate Scheme **(b)** Seed-multiply-Add-Accumulate Scheme

Input a(x), b(x), f (x)
Output D(x) =a(x) b(x) x^{-k}mod f (x)
1. D(x) = 0
2. For i=0 to k-1 do begin
3. D(x) = D(x) + a_i b(x)
4. D(x) =D (x) + D_0 f(x)
5. D(x) = D(x)/ x
End
6. Return D(x)

Algorithm.1: Galois based Finite field multiplier algorithm

Simulation Analysis and Results Discussion:
Xilinx/ISE Simulations:

The algorithms were all simulated in Xilinx. The proposed techniques will be simulated, implemented and validated in high end Virtex-6 low power FPGA's of 45nm technology.

In order to prove the effectiveness of the proposed scheme, first, we simulated the proposed method with the specific fault non-detectable period. We compared the fault coverage of the test patterns generated by LFSRs, MSIC and by the proposed method using the GBMAC. The proposed scheme has a higher fault coverage with fewer test patterns for all circuits except two the proposed scheme has a fault coverage similar to that of the conventional method using LFSRs, MSIC. Al-though some of the circuits show a little bit less fault coverage, the fault coverage degradation is very small. For most circuits, the test patterns obtained by the proposed method provide proper fault coverage compared to the conventional method using LFSRs and MSIC. For a better comparison, of all the performance parameter are analyzed In the results, test patterns generated by the proposed method using the GB-MAC can effectively produce pattern generator the proposed scheme can generate Test pattern sequences without fault coverage degradation compared with the conventional method using an LFSR, MSIC.

Table I: Parameter comparison for conventional and proposed method.

Logic Utilization	GBMAC	MSIC	LFSR	Available
Number of Slices	3	9	13	2448
Number of Slice Flip Flops	5	16	5	4896
Number of 4 input LUTs	1	1	24	4896
Number of bonded IOBs	7	18	18	158
Number of GCLKs	1	1	1	24
Selected Device:3s250epq208-4				

Table I and Table II summarizes the performance of the proposed scheme compared with the conventional LFSR in terms of area and delay scheme. The fault coverage of the proposed scheme is 5 % higher than that of the conventional scheme on average.

Table II: Path and Delay comparison for conventional and proposed method.

Parameters	GBMAC	MSIC	LFSR
Delay	2.225ns (Maximum frequency: 449.438MHz)	3.449ns (Maximum Frequency: 289.914MHz)	2.225ns (Maximum Frequency: 449.438MHz)
Total number of paths / destination ports:	6 / 5	17 / 5	19 / 16
Total CPU time to Xst completion	3.75 secs	3.92 secs	3.84 secs
Power(W)	1.8	2.2	2.7

As shown in the Table II. The conventional approach and the proposed GBMAC is analyzed based on the cost function of total number of paths and destination ports and CPU time completion for processing the architecture. As number of LUT's and CLB's are reduced in proposed flow due to less consumption of adder circuit in the design which designing multiplier based on Galois approach. We can see that the conventional approach increases the critical path delay by 3.449ns (in the case of the minimum route channel width) and produce 13.774ns combinational path **,**while the proposed GBMAC increases the critical path delay by 2.225ns respectively. In terms of overhead, since the conventional approach and the proposed method only change the placement and routing of the design, as the usage of the LUT (Look up table) which terms to be characteristic memory element inside CLB(configurable logic block) (As shown in the Table.III, IV and V) (Xijiang Lin., Rajski, J., Dec 2010)

Table III: Cell usage (LUT's) for MSIC.

Cell Usage :	
# BELS	24
# LUT2	4
# LUT3	4
# LUT4	13
# LUT4_D	1
# LUT4_L	2
# Flip-flops/Latches	5
# FDP	5
# IO Buffers	17
# IBUF	7
# OBUF	10

(Configurable logic blocks) varies which provides the overhead and power consumption lesser than existing approach.

Table III: Cell usage (LUT's) for MAC

Cell Usage:	
# BELS	1
# LUT2	1
# Flip-flops/Latches	5
# FDP	5
# IO Buffers	6
# IBUF	1
# OBUF	9

Table IV: Cell usage (LUT's) for LFSR.

Cell Usage :	
# BELS	1
# LUT4	1
# Flip-flops/Latches	16
# FDC	15
# FDP	1

# Clock Buffers	1
# BUFGP	1
# IO Buffers	17
# IBUF	1
# OBUF	16

A comparison of, newly developed test solutions with respect to key parameters of low power testing like, test power, delay and so on is presented for choosing a best possible solution. This proposed method utilizes GBMAC (multiply and accumulate) units, which consist of Galois based-Finite field Multipliers combined several accumulators, to generate test patterns in DSP. Hence the new method can generate test patterns without LFSRs (linear feedback shift registers) and Multiple Single Input Change (MSIC).

Conclusion:

A new multiplicative two-dimensional test pattern generation scheme has been proposed in this paper. The scheme can b e used to test less regular parts of circuits accessible through scan, parallel scan, partial scan, or boundary scan chains. All processors and circuits have self-test circuits. How-ever, the conventional self-test circuits, such as BIST using LFSRs, have effective fault coverage, but require an additional hardware. In this paper, the proposed GBMAC to be used as a pseudo-random test-pattern generator. The superiority of Galois based generators(GBMAC) over traditionally used linear feedback shift registers is clearly pronounced by experimental results indicating much higher capability to provide desired vector patterns on selected positions in scan registers. The simulation results shows that the GB- MAC is suitable for test-pattern generation and can achieve high fault coverage. In addition, the new method requires a smaller hardware overhead than the conventional method. A comparison of, newly developed test solutions outperforms the conventional method in-terms of test power with 22%-33% reduction, 35% reduction in delay and 68% reduction in area overhead.

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